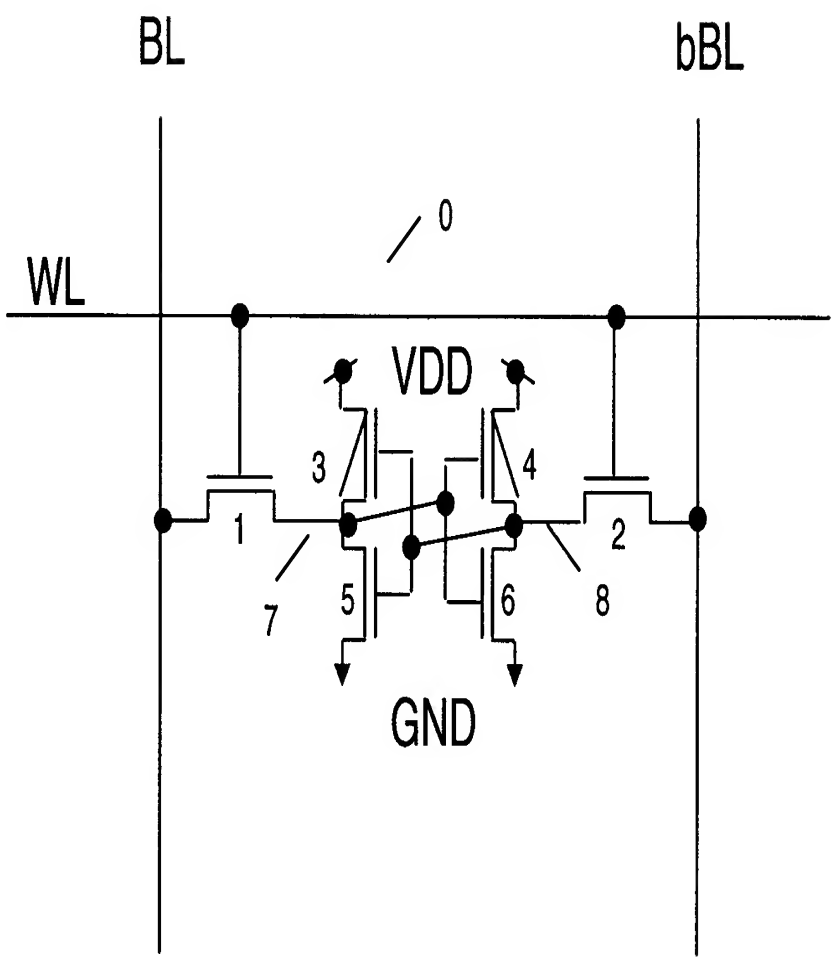


FIG. 1(A) (PRIOR ART)

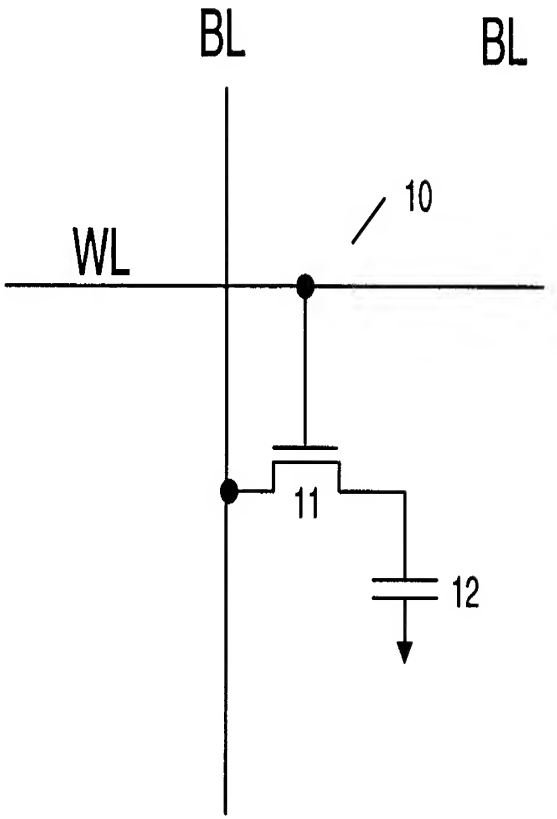


FIG. 1(B) (PRIOR ART)

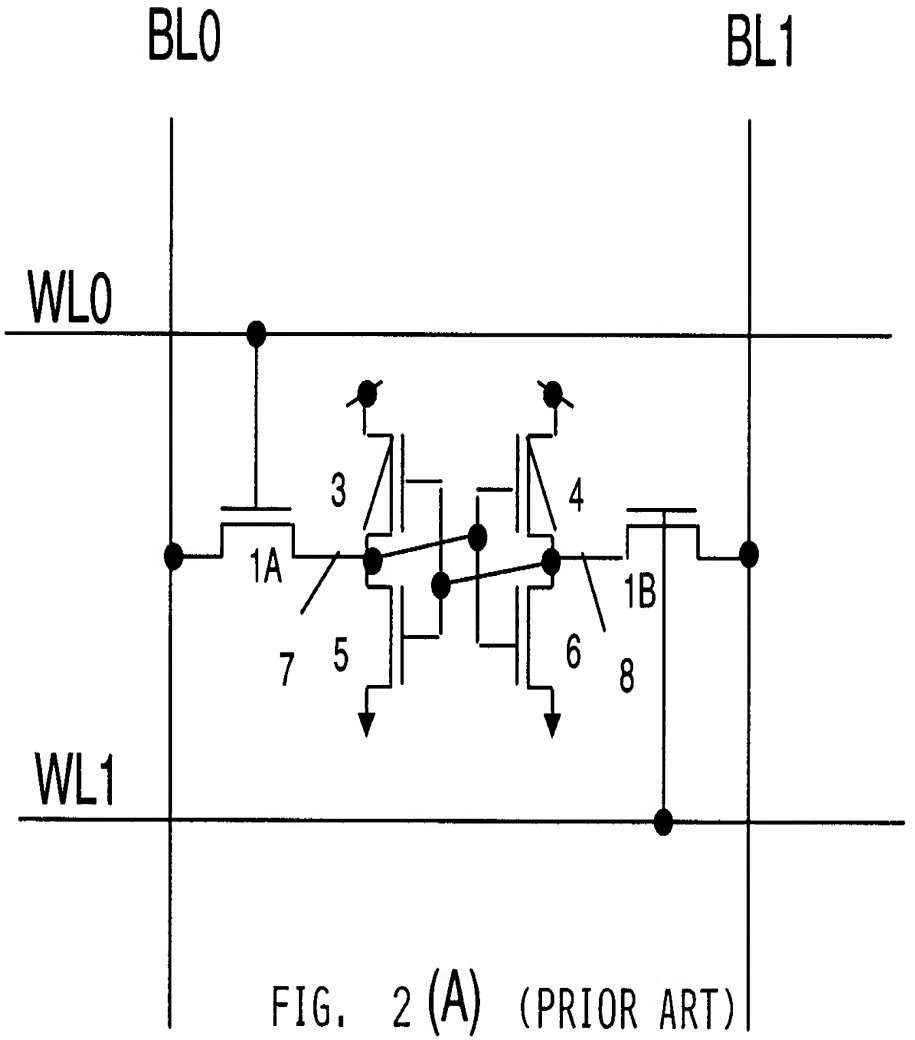


FIG. 2 (A) (PRIOR ART)

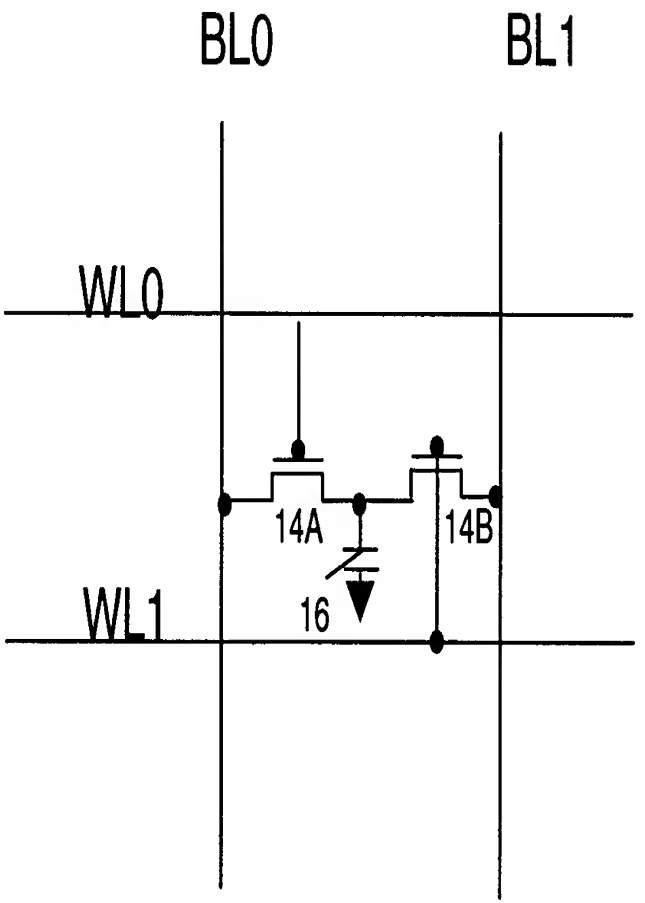


FIG. 2 (B) (PRIOR ART)

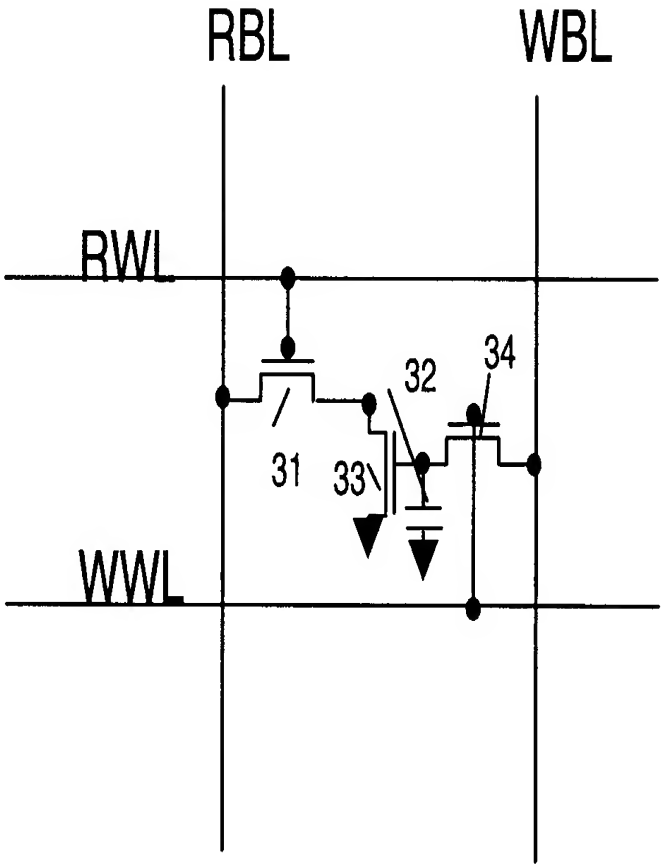


FIG. 3(A) (PRIOR ART)

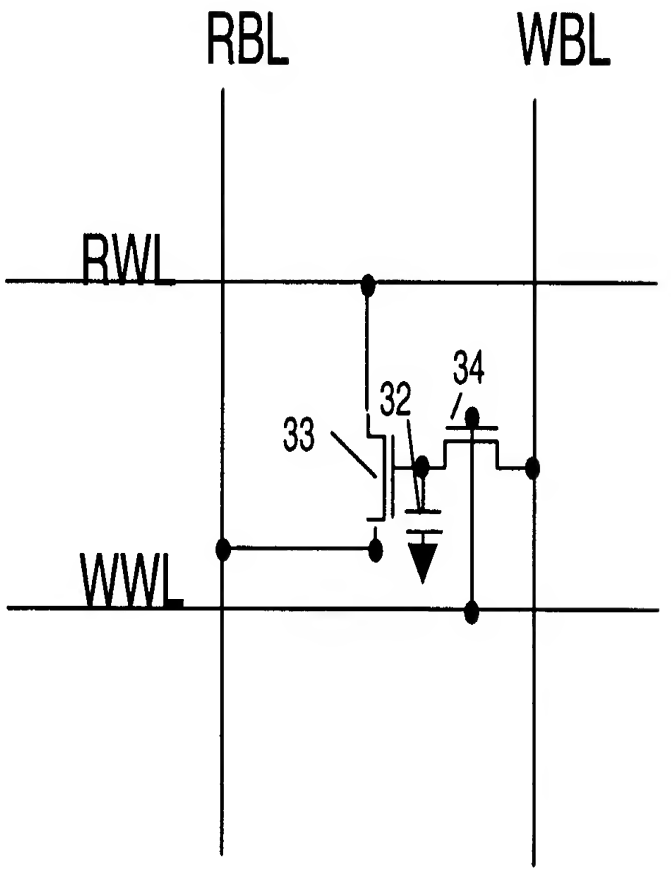


FIG. 3(B) (PRIOR ART)

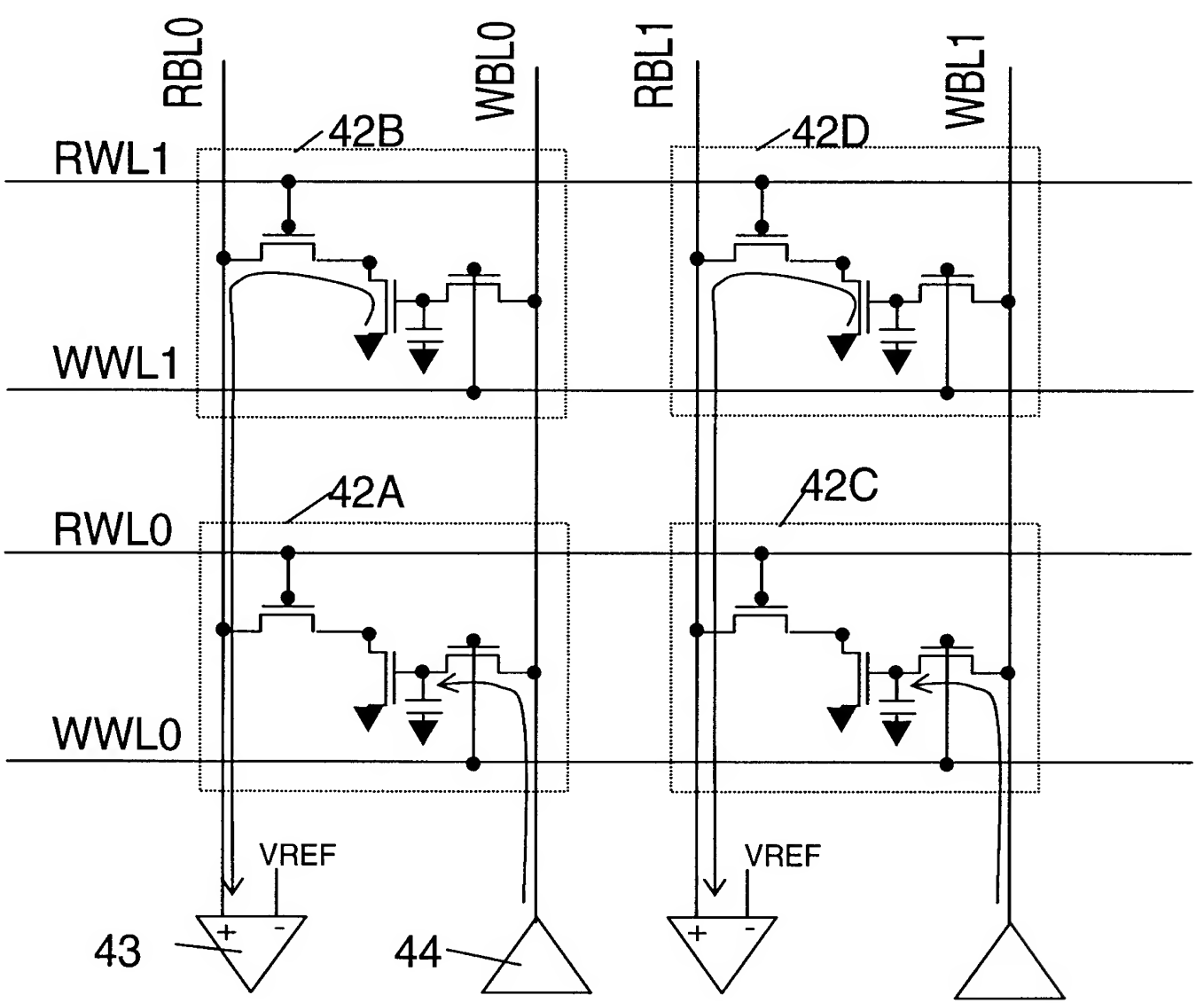
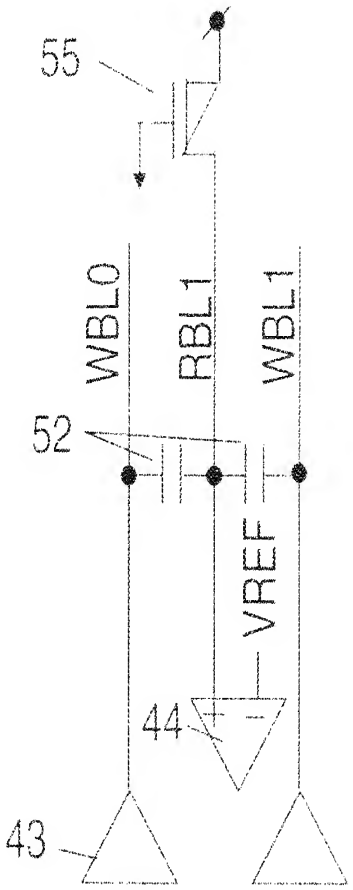


Fig. 4 (PRIOR ART)



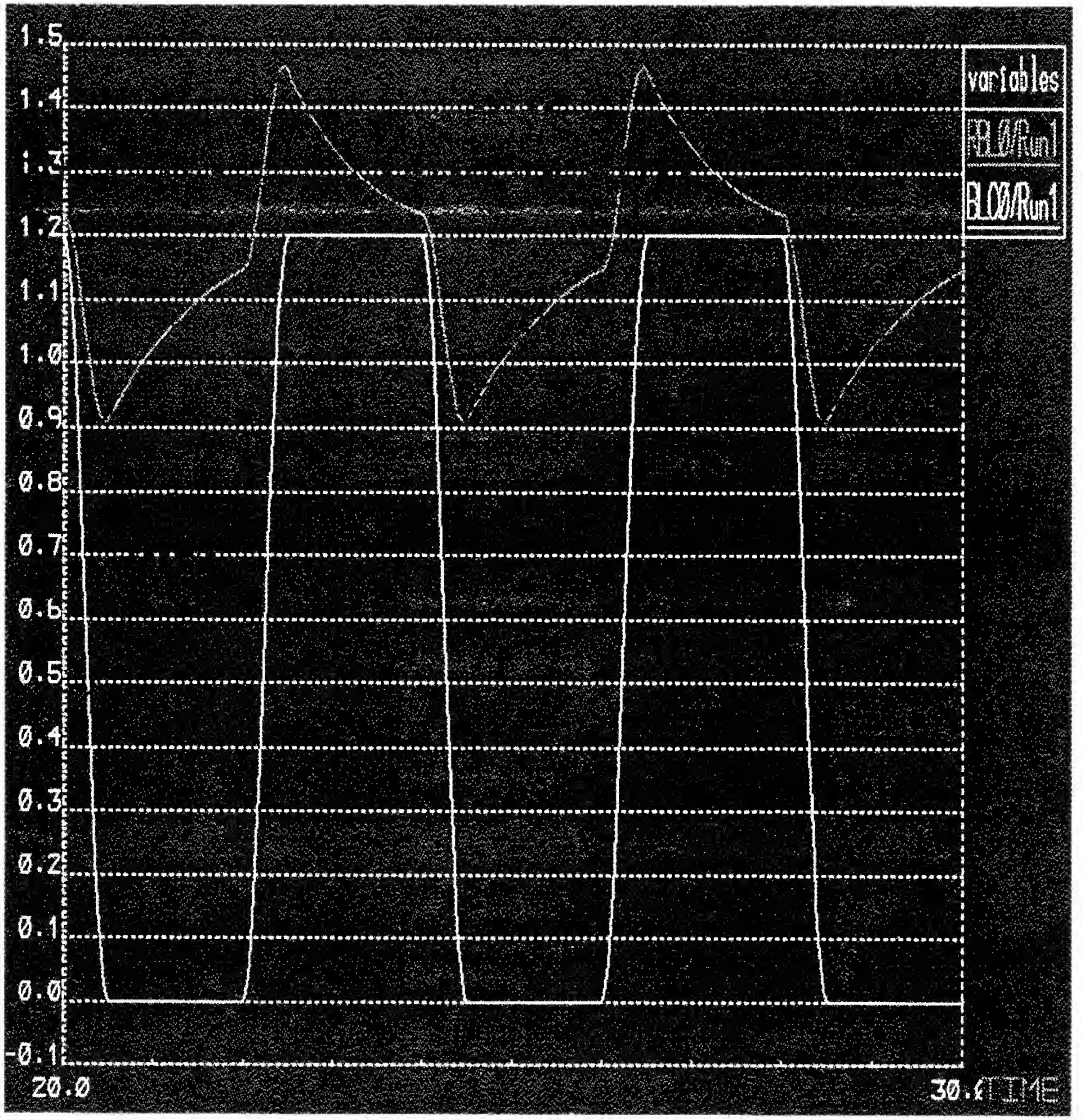


Fig. 5 (PRIOR ART)

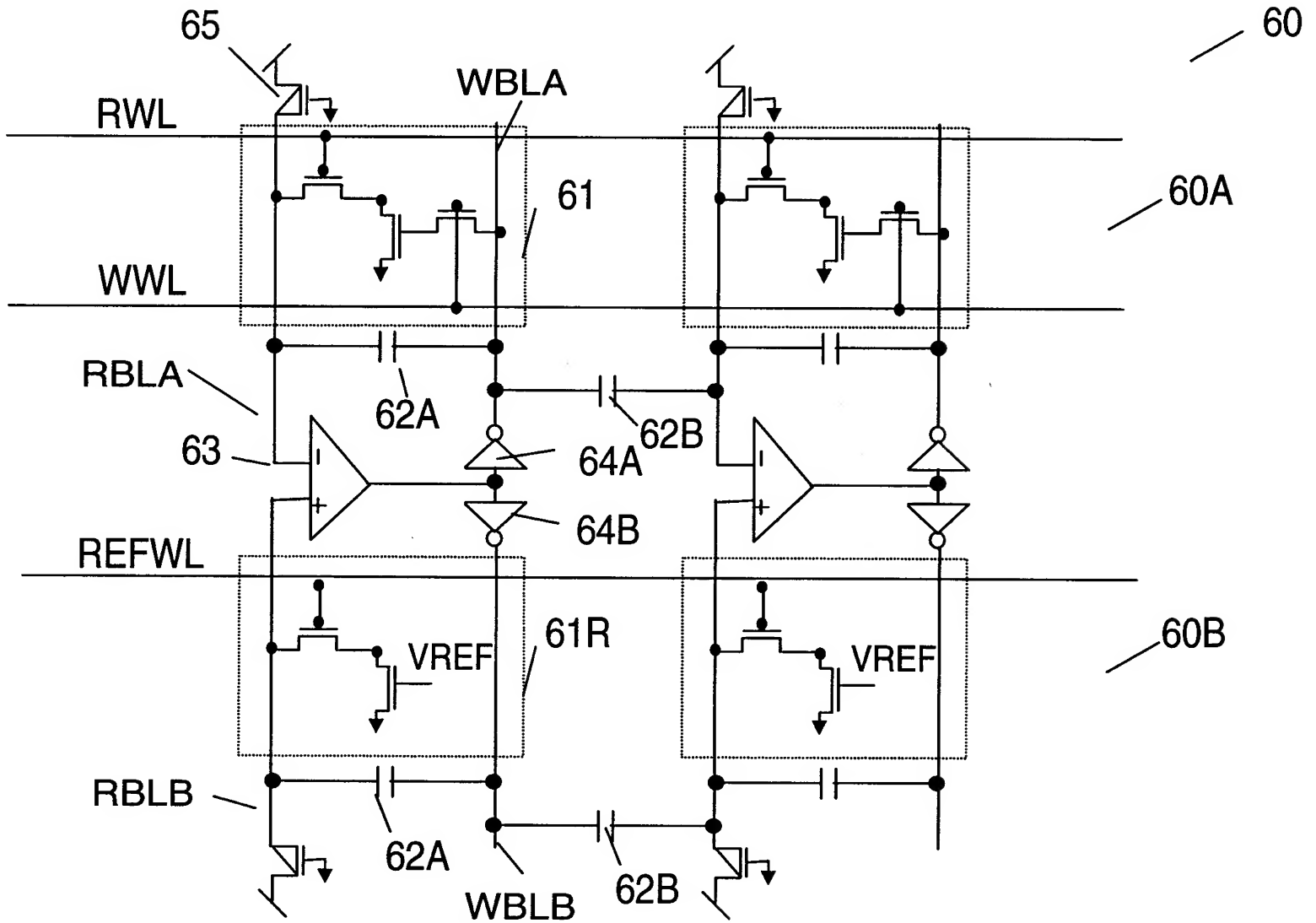

65
60
WBLA
RWL
61
60A
WWL
RBLA
62A
62B
63
64A
64B
REFWL
61R
VREF
VREF
60B
RBLB
62A
WBLB
62B

Fig. 6

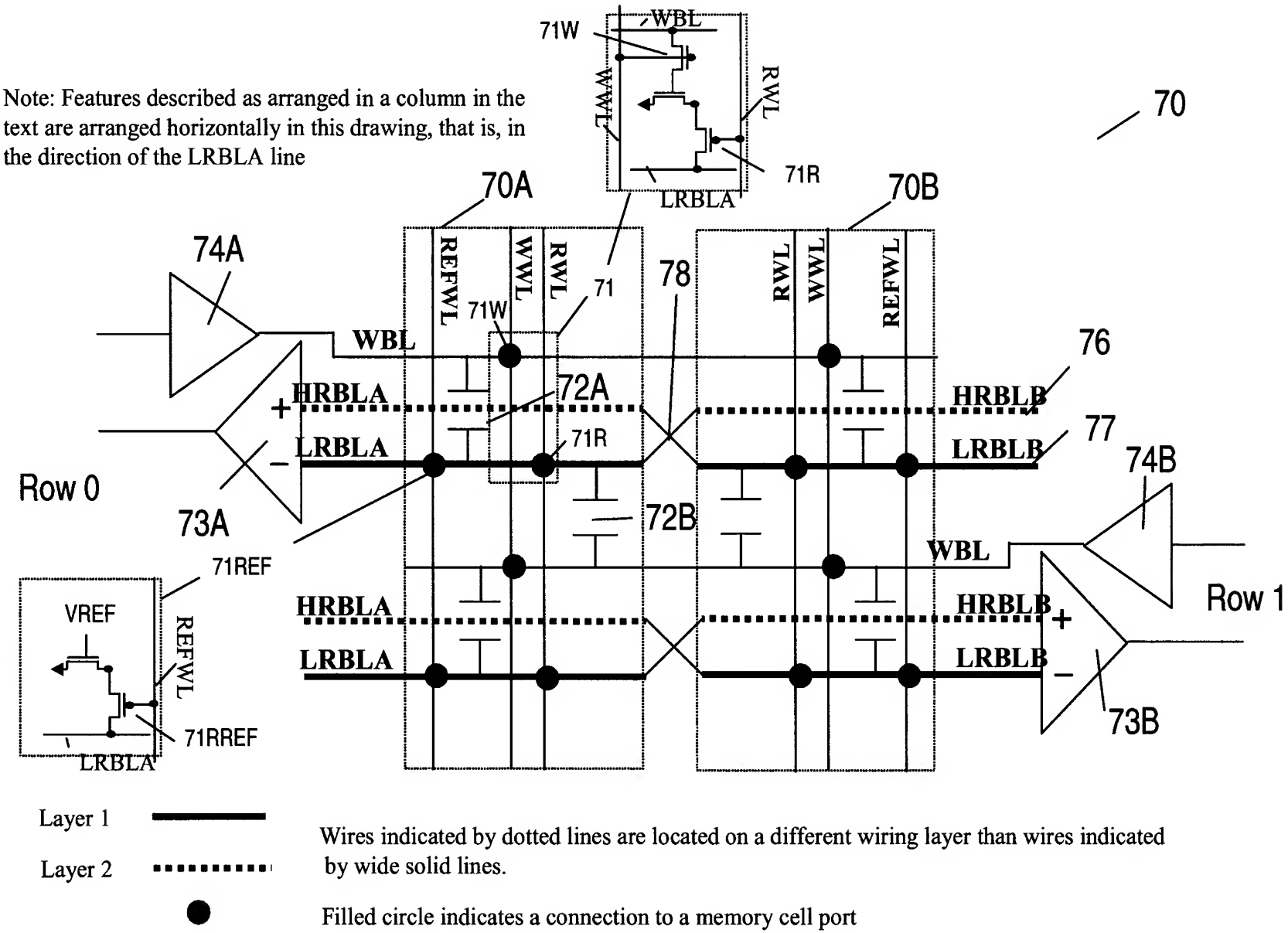
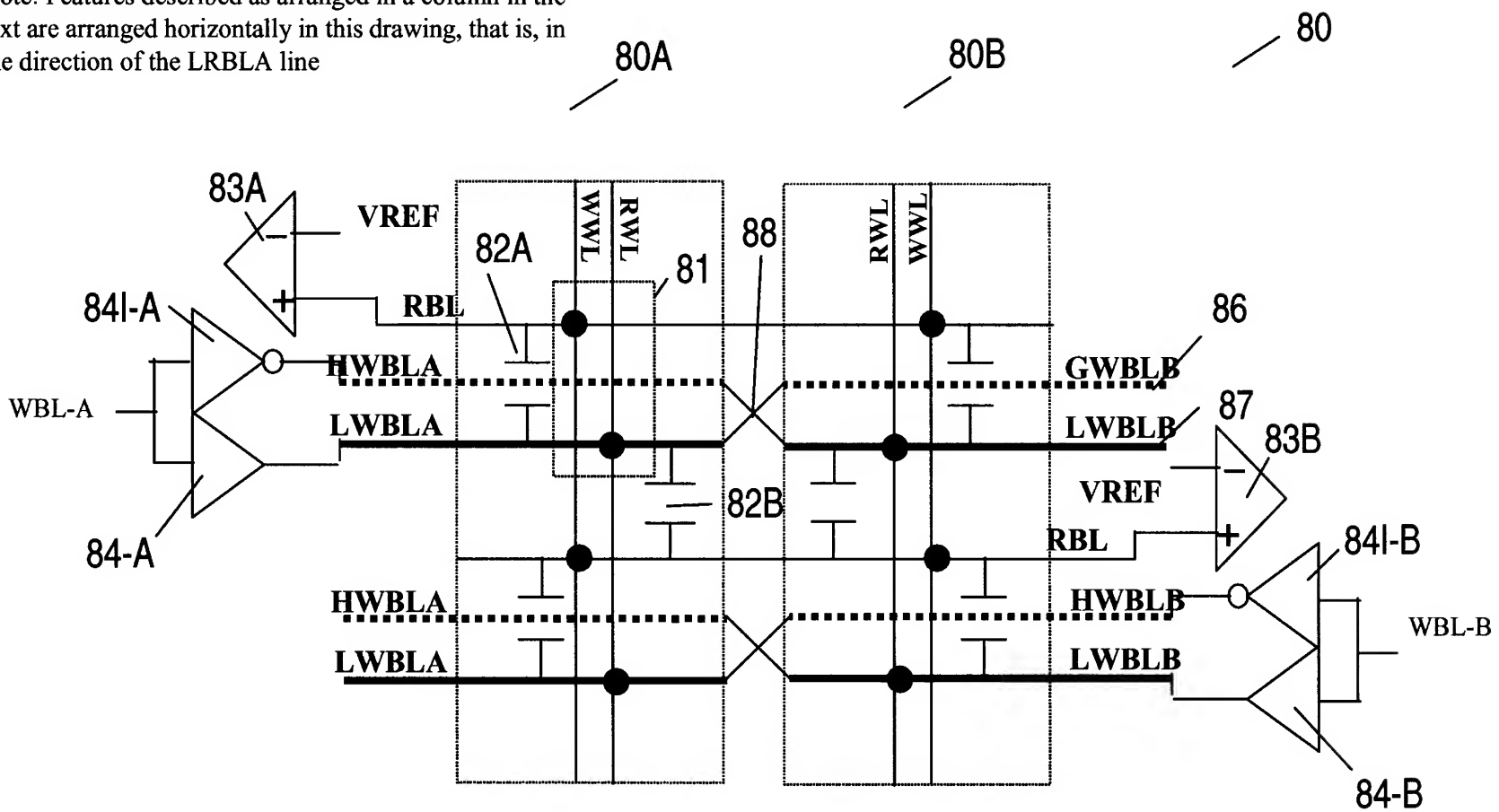

Note: Features described as arranged in a column in the text are arranged horizontally in this drawing, that is, in the direction of the LRBLA line
71W
WBL
WWL
RWL
71R
LRBLA
70
70A
70B
74A
REFWL
WWL
RWL
71
78
RWL
WWL
REFWL
71W
WBL
76
HRBLA
72A
HRBLB
+
LRBLA
71R
LRBLB
77
74B
Row 0
73A
72B
WBL
71REF
VREF
REFWL
HRBLA
HRBLB
Row 1
+
LRBLA
LRBLB
71RREF
LRBLA
73B
Layer 1
Layer 2
Wires indicated by dotted lines are located on a different wiring layer than wires indicated by wide solid lines.
Filled circle indicates a connection to a memory cell port

Fig. 7

Note: Features described as arranged in a column in the text are arranged horizontally in this drawing, that is, in the direction of the LRBLA line



Layer 1 ——————

Layer 2 ....

Wires indicated by dotted lines are located on a different wiring layer than wires indicated by solid lines

Fig. 8